REMARKS

Reconsideration is respectfully requested.

By the above amendments, a substitute specification is submitted, as set forth in the attached pages, together with a marked up copy of the specification to show the amendments made thereto. These amendments are intended to provide to the specification English idiomatic expression and to correct for the typographical inconsistency regarding the data odd pad 17a, and the data even pad 17b. No new matter has been added by these amendments.

With respect to the requirements for drawing amendments, attached hereto are drawing corrections to include the identification of a data odd pad 17a and a data even pad 17b. The additional amendments to the specification, see above, have also corrected for the typographical inconsistency of the data odd pad and data even pad connections, as noted.

New drawing FIGS. 3B, 4A and 4B have been proposed to correct for the previously noted discrepancies in the odd and even data pads, for which the Examiner's approval is respectfully requested. Marked up drawings showing the corrections are also attached.

With respect to the rejection of Claims 9-12 based on U.S.C. § 112, first paragraph, it is noted that Figs. 3A and 3B are related, as Fig. 3B is a detail of the corner part of the TFT array shown in Fig. 3A. Figs. 4A and 4B are also detail views of the corner part, in which Fig. 4A shows a disconnection in the wiring and Fig. 4B shows a short thereof. As illustrated, the TFT in Fig. 3A is shown in a schematic diagram, with only a few pixels, out of the large number that would normally appear in such an array; for example, 100 pixels per square centimeter is not uncommon and one million pixels in an array is feasible. Thus, the pixels between say D5 through Dn are shown schematically and are represented by ellipses (...).

Thus for example, Claim 9 includes elements that are each illustrated in the drawing figures without requiring each and every pixel in an array to be shown. The statement that the structure

recited in Claims 9-12 "requires the formation of pixels in the TFT array" is correct, and such structure is shown in which each pixel is defined by the adjacent data lines Dn and D(n+1) and gate lines Gn and G(n+1). The TFT is formed within the pixel bounded by these lines, as is shown.

With respect to the prior art rejections, it is respectfully suggested that the Applicants Admitted Prior Art (AAPA), as shown in Figs. 1 and 2, fails to anticipate Claims 1-3, 5-7, and 9-11 in that each limitation recited in at least independent Claims 1, 5 and 9 is not taught or otherwise suggested by the AAPA, for the AAPA fails to show the limitation by which "the wiring unit for testing defects of the data line being connected between the data pad unit and the data line," (emphasis added). In contradistinction, and as set forth at page 2, lines 8-14 of the originally filed specification, (page 1, line 19 through page 2, line 2 of the attached substitute specification), the wiring is formed "on the corner of the upper part of panel 10," without a direct interconnection to the dataline, gate line or common voltage line, as is recited in, respectively, Claims 1, 5 and 9. Thus, it is respectfully suggested that the rejection of Claims 1-3, 5-7, and 9-11 is improper.

The AAPA also fails to show the wiring unit for testing defects of the data line or gate line which is connected in series between the data pad unit and the data line, or between the gate pad unit and the gate line, respectively. In addition, the feature of the present invention is in not simply the zigzag shape of the wiring unit, but the existence of the wiring unit for testing defects of the data line or gate line, being formed in a zigzag shape. Chung et al. merely discloses an LCD apparatus comprising stitch defect correcting elements included in the data lines or gate lines, to eliminate stitching defects caused by an irregularity in a width of a gate line or data line, and does not disclose or suggest any attempts to test defects that may be present in panel wiring in a FPC or PCB less module. Therefore, the present inventions as claimed in claims 1 to 12 are novel and non-obvious over the AAPA in view of Chung et al.

Similarly, the rejection of Claims 4, 8 and 12 is also improper in that the combination of AAPA and Chung et al. fail to set forth a *prima facie* case of obviousness, because as set forth above with respect to independent Claims 1-3, 5-7 and 9-11, the same recited limitation is missing from the proposed combination. Chung et al. fail to provide this missing element, and it is not obvious to include the zigzag structure in the AAPA as suggested. Moreover, the incentive identified by Chung et al., to correct for the "stitching defect" is not relevant to the modification of the AAPA device simply because the "stitching defect" does not appear to be a consideration in the present invention or in the AAPA. As set forth in the specification at page 10, lines 12-17, the wiring pattern shape is formed in the inventive TFT array so that the wiring provides means for quick and easy determination of short or disconnection anomalies, which can be used for testing integrity of the connections. This does not relate to any "stitching defect," and as such, a teaching, suggestion or incentive to perform the modification as proposed in the rejection is lacking.

For the above reasons, it is considered that the claims, as amended, find support in the application specification as filed, and that the combination of elements recited in the pending claims, as amended, distinguish over the references of record. Accordingly, reconsideration and withdrawal of the outstanding rejections are respectfully requested an indication of allowable subject matter is earnestly solicited.

Respectfully submitted,

January 20, 2004

Vangelis Economou -Reg. No. 32,341
c/o Ladas & Parry
224 South Michigan Avenue - Suite 1200
Chicago Illinois 60604
Tel. No. (312) 427-1300